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EXAMINER	
IWASHKO, LEV	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,893	LIN, AKAN	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-5 and 7-10 are rejected under U.S.C. 102(e) as being anticipated by Mathews (US Patent 6,625,715).

Claim 1. A method of determining whether a virtual address corresponds to a physical address in a translation lookaside buffer (TLB),

- the virtual address comprising a plurality of bits,the translation lookaside buffer (TLB) comprising a plurality of tag addresses and page types, and the physical addresses corresponding to each tag address, the method comprising: *(Column 14, lines 10-37 – State the following: "FIG. 11 is a block diagram of one embodiment of a method 1100 of translating virtual addresses of varying page sizes to physical addresses. Method 1100 begins and thereafter generates an entry select 1110. The entry select is a pointer into two arrays that*

identifies a set of corresponding entries (one entry in each array), where the first array such as 740 in FIG. 7, maps the virtual page address such as 430 and 440 in FIG. 4, to a physical page address 1120, such as 540 in FIG. 5, and generates a virtual address tag such as 770 in FIG. 7, and the second array, such as 750 in FIG. 7, generates a match indication such as match signal 758 in FIG. 7. The second array generates its match signal if the entry in the second array selected by the entry select is valid (as indicated by a valid bit such as 756 in FIG. 7), and the variable page address such as 730 in FIG. 7 (after being masked by the page size mask, such as 754 in FIG. 7, selected by the entry select) matches the virtual address tag such as 752 in FIG. 7 selected by the entry select (after being masked by the page size mask, such as 754 in FIG. 7, selected by the entry select). A match 1130 is indicated when both the second array indicates a match, and the virtual address tag from the first array is determined to be equal to the virtual fixed page address input such as 790 in FIG. 7. If a match is indicated, then the physical address is generated 1140 by concatenating the physical page address such as 540 in FIG. 5 with the offset from the virtual address, such as 520 in FIG. 5. and the physical address is used to access physical memory, such as 130 in FIG. 1, thereafter method 1100 ends.")

- (a) receiving the virtual address; *(Column 2, lines 55-57 – State the following: "In one embodiment of a method of the present invention, the system receives a virtual address")*
- (b) setting the page type of the virtual address according to the rank of the page types; *(Column 2, lines 59-63 – State the following: "The page size bias is used in the look-up of the physical address. During intermediate stages of the virtual to physical address translation, according to the look-up of the virtual address and page size bias, a page size mask and physical page address are generated.")*

- (c) fetching index bits and a tag compared address from the page type; *(Column 10, lines 22-31 – State the following: "These entry selects correspond to the entry selects shown in FIG. 7 used to index the RAM array 740 and CAM array 780. When in operation, first, the page size bias 810 is ANDed with (used to mask) the lower bits of the variable page address 820. Then the AND gate output is XORed with the next higher contiguous set of bits in the variable page address 820, in order to hash the masked variable page address 820. Lastly, the hash output is decoded, resulting in the generation of the entry selects.")*
- (d) comparing the page type of the virtual address in step (b) and the tag compared address in step (c) with the page types and the tag addresses in the TLB; and *(Column 11, lines 6-9 – State the following: "Each physical address tag generated from cache tag 930 is compared to the physical address generated by each of the translation buffers of the TLB and masked with the TLB match signals for determine which way of the cache was hit.")*
- (e) determining the rank of the page type if the page type of the virtual address in step (b) and the tag compared bits in step (c) correspond with a page type and a tag address in the TLB. *(Column 15, lines 29-44 – State the following: "FIG. 15 is a block diagram of one embodiment of a method 1500 of generating a physical page address as in action 1120 in FIG. 11 and action 1220 in FIG. 12. In general, a physical page address is generated by combining a portion of the physical page address contained within the translation buffer with a portion of the variable page address input as indicated by the page size contained within the translation buffer. More specifically, the lower portion of the physical page address contained within the translation buffer is masked off according to the page size contained within the translation buffer to the extent that those bits which would be considered offset within the page (as opposed to the address of the*

page within memory space) are masked. Those masked bits are then replaced with the corresponding bits of the variable page address input to generate the physical page address output.")

Claim 2. The method of claim 1 further comprising searching for a page type in the TLB corresponding to the set page type of the virtual address and an index address for comparing the page type with the tag compared address according to the index bits of the virtual address. *(Column 7, lines 44-51 – State the following: "Conventionally, a TLB 150 in FIG. 1 in computer system 100 will use only one page size, such as a 4K page size as in FIG.2 or a 256K page size as in FIG. 3 to translate a virtual address word 200 as in FIG. 2 or virtual address word 300 as in FIG. 3 into a physical address word 500 as in FIG. 5 or require a TLB for each pages size supported. However, the inventive system overcomes this problem by enabling a single TLB to implement two or more page sizes.")*

Claim 3. The method of claim 1 wherein determining the rank of the page type in step (e) comprises raising the rank of the page type of the virtual address if the page type of the virtual address set in step (b) corresponds with a page type in the TLB, if the tag compared address in step (c) corresponds with the tag address in the TLB, and if the rank of the page type of the virtual address in step (b) is not the highest. *(Column 7, lines 53-67 and Column 8, lines 1-11 – State the following: "FIG. 6 is a block diagram of one embodiment of the present invention. System 600 includes a TLB 610 that accepts an input virtual address 620 and an input indication of a page size bias 630. The TLB translates the input virtual address 620 into an output physical address 640 if the input virtual address 620 matched an entry in the TLB 610, otherwise, an indication of a TLB miss 650 is transmitted. A more detailed description of TLB 610 is described with reference to FIGS. 7-10. FIG. 7 is a block diagram of one embodiment of the translation buffer 700 of the present invention. The decoder 710 receives the page size bias 720, which corresponds to TLB 610 that accepts an input*

indication of a page size bias 630. The page size bias 720 is a set of bits that is as wide as minimally necessary to describe the range from the smallest page size to the largest page size that the translation buffer will support. In one embodiment, the page size bias will be 6 bits wide in order to describe seven page sizes ranging from 4K as in virtual address word 200 in FIG. 2 to 256K as in virtual address word 300 in FIG. 3. In one embodiment of the page size bias 720, a programmable register is implemented to select the value of the bias. In another embodiment of the page size bias 720, a set of programmable registers are implemented to select the value of the bias based upon the current privilege level (CPL) of the program.")

Claim 4. The method of claim 3 wherein the rank of the page type of the virtual address is raised by one level if the page type of the virtual address set in step (b) corresponds with a page type in the TLB, if the tag compared address in step (c) corresponds with the tag address in the TLB, and if the rank of the page type of the virtual address in step (b) is not the highest. *(Column 7, lines 53-67 and Column 8, lines 1-11 – State the following: "FIG. 6 is a block diagram of one embodiment of the present invention. System 600 includes a TLB 610 that accepts an input virtual address 620 and an input indication of a page size bias 630. The TLB translates the input virtual address 620 into an output physical address 640 if the input virtual address 620 matched an entry in the TLB 610, otherwise, an indication of a TLB miss 650 is transmitted. A more detailed description of TLB 610 is described with reference to FIGS. 7-10. FIG. 7 is a block diagram of one embodiment of the translation buffer 700 of the present invention. The decoder 710 receives the page size bias 720, which corresponds to TLB 610 that accepts an input indication of a page size bias 630. The page size bias 720 is a set of bits that is as wide as minimally necessary to describe the range from the smallest page size to the largest page size that the translation buffer will support. In one*

embodiment, the page size bias will be 6 bits wide in order to describe seven page sizes ranging from 4K as in virtual address word 200 in FIG. 2 to 256K as in virtual address word 300 in FIG. 3. In one embodiment of the page size bias 720, a programmable register is implemented to select the value of the bias. In another embodiment of the page size bias 720, a set of programmable registers are implemented to select the value of the bias based upon the current privilege level (CPL) of the program.")

Claim 5. The method of claim 1 wherein determining the rank of the page type in step (e) comprises following steps:

- (i) calculating a number of times in which the set page type of the virtual address in step (b) corresponds with a page type in the TLB; and (ii) raising the rank of the page type according to the calculated number. *(Column 9, lines 18-30 – State the following: "In another embodiment in which not all possible page sizes between the smallest page size implemented and the largest page size implemented are supported, the page mask bits 744 may be reduced and have a many-to-1 correspondence with respect to the variable page address 730, and the physical page address 746. For example, in an embodiment in which the only page sizes of the virtual address supported by the RAM array 740, are 4K and 256M, then a single page mask bit 744 corresponding to virtual address bits 12-27 may be used to indicate whether bits 12-27 of the output physical page address 760, would come from the variable page address 730 or the physical page address 746 selected.")*

Claim 7. The method of claim 1 wherein setting the page type of the virtual address according to the rank of the page type in step (b) comprises setting the page type of the virtual address to be a page type with higher rank. *(Column 10, lines 22-31 – State the following: "These entry selects correspond to the entry selects shown in FIG. 7 used to index the RAM array 740 and CAM array 780. When in operation, first, the page size*

bias 810 is ANDed with (used to mask) the lower bits of the variable page address 820. Then the AND gate output is XORed with the next higher contiguous set of bits in the variable page address 820, in order to hash the masked variable page address 820. Lastly, the hash output is decoded, resulting in the generation of the entry selects.")

Claim 8. A determining device for determining whether a virtual address corresponds to a physical address in a TLB, comprising:

- a mask selecting module used for receiving the virtual address and outputting a part of the bits of the virtual address and a page type signal according to a rank of a page type; *(Column 3, lines 63-67 and Column 4, lines 1-6 – State the following: "It then uses the entry selects to select an entry and masks the variable page address supplied with the page size mask of the entry selected such that the portion of the variable page address which corresponds to the offset address within the page is masked and compares this result for equality with the variable virtual address tag of the entry selected, similarly masked with the page size mask of the entry selected, to generate match signal (the match signal is also qualified with a valid bit contained within the second array which indicates whether or not the translation buffer entry selected is valid).")*
- a translation lookaside module comprising: a TLB used for storing a plurality of index addresses and a plurality of page types; *(Column 16, lines 37-40 – State the following: "If a comparison of the virtual fixed address tag and the virtual fixed address input 1650 indicates inequality, then an indication of no match is output 1620, and the method ends.")*
- a tag address comparing module used for checking whether the part of bits outputted by the mask selecting module corresponds with an index stored in the TLB; *(Column 14, lines 10-37 – State the following: "FIG. 11 is a block diagram of one embodiment of a method 1100 of*

translating virtual addresses of varying page sizes to physical addresses. Method 1100 begins and thereafter generates an entry select 1110. The entry select is a pointer into two arrays that identifies a set of corresponding entries (one entry in each array), where the first array such as 740 in FIG. 7, maps the virtual page address such as 430 and 440 in FIG. 4, to a physical page address 1120, such as 540 in FIG. 5, and generates a virtual address tag such as 770 in FIG. 7, and the second array, such as 750 in FIG. 7, generates a match indication such as match signal 758 in FIG. 7. The second array generates its match signal if the entry in the second array selected by the entry select is valid (as indicated by a valid bit such as 756 in FIG. 7), and the variable page address such as 730 in FIG. 7 (after being masked by the page size mask, such as 754 in FIG. 7, selected by the entry select) matches the virtual address tag such as 752 in FIG. 7 selected by the entry select (after being masked by the page size mask, such as 754 in FIG. 7, selected by the entry select). A match 1130 is indicated when both the second array indicates a match, and the virtual address tag from the first array is determined to be equal to the virtual fixed page address input such as 790 in FIG. 7. If a match is indicated, then the physical address is generated 1140 by concatenating the physical page address such as 540 in FIG. 5 with the offset from the virtual address, such as 520 in FIG. 5. and the physical address is used to access physical memory, such as 130 in FIG. 1, thereafter method 1100 ends.")

- and a page type comparing module used for checking whether the page type signal outputted by the mask selecting module corresponds with a page type stored in the TLB; *(Column 14, lines 60-63 – State the following: "FIG. 13 is a block diagram of one embodiment of a method 1300 of generating an entry select as in action 1110 in FIG.*

11, in the translation of virtual addresses of varying page sizes to physical addresses.")

- and a rank generating module used for generating the ranks of the plurality of the page types in the TLB according to the checking result of the page type comparing module. *(Column 15, lines 29-44 – State the following: "FIG. 15 is a block diagram of one embodiment of a method 1500 of generating a physical page address as in action 1120 in FIG. 11 and action 1220 in FIG. 12. In general, a physical page address is generated by combining a portion of the physical page address contained within the translation buffer with a portion of the variable page address input as indicated by the page size contained within the translation buffer. More specifically, the lower portion of the physical page address contained within the translation buffer is masked off according to the page size contained within the translation buffer to the extent that those bits which would be considered offset within the page (as opposed to the address of the page within memory space) are masked. Those masked bits are then replaced with the corresponding bits of the variable page address input to generate the physical page address output.")*

Claim 9. The determining device of claim 8 wherein the rank generating module sets the ranks of the page types in the TLB according to the number of times the page type signal corresponds to the one of the page types in the TLB. *(Column 9, lines 18-30 – State the following: "In another embodiment in which not all possible page sizes between the smallest page size implemented and the largest page size implemented are supported, the page mask bits 744 may be reduced and have a many-to-1 correspondence with respect to the variable page address 730, and the physical page address 746. For example, in an embodiment in which the only page sizes of the virtual address supported by the RAM array 740, are 4K and 256M, then a single page mask bit 744 corresponding to virtual address bits 12-*

27 may be used to indicate whether bits 12-27 of the output physical page address 760, would come from the variable page address 730 or the physical page address 746 selected.")

Claim 10. The determining device of claim 8 wherein the rank generating module is used for raising the rank of the page types in the TLB if the page type signal corresponds to the one of the page types in the TLB and if the corresponding rank of the page type is not the highest. *(Column 7, lines 53-67 and Column 8, lines 1-11 – State the following: "FIG. 6 is a block diagram of one embodiment of the present invention. System 600 includes a TLB 610 that accepts an input virtual address 620 and an input indication of a page size bias 630. The TLB translates the input virtual address 620 into an output physical address 640 if the input virtual address 620 matched an entry in the TLB 610, otherwise, an indication of a TLB miss 650 is transmitted. A more detailed description of TLB 610 is described with reference to FIGS. 7-10. FIG. 7 is a block diagram of one embodiment of the translation buffer 700 of the present invention. The decoder 710 receives the page size bias 720, which corresponds to TLB 610 that accepts an input indication of a page size bias 630. The page size bias 720 is a set of bits that is as wide as minimally necessary to describe the range from the smallest page size to the largest page size that the translation buffer will support. In one embodiment, the page size bias will be 6 bits wide in order to describe seven page sizes ranging from 4K as in virtual address word 200 in FIG. 2 to 256K as in virtual address word 300 in FIG. 3. In one embodiment of the page size bias 720, a programmable register is implemented to select the value of the bias. In another embodiment of the page size bias 720, a set of programmable registers are implemented to select the value of the bias based upon the current privilege level (CPL) of the program.")*

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 6 is rejected under 35 U.S.C.103(a) as being unpatentable over Mathews as applied to claim 1 above, further in view of McFarland et al. (US Patent 4,595,923).

Mathews teaches the limitations of claims 1 and 4 for the reasons above.

Mathews' invention differs from the claimed invention in that there is no specific reference dividing the local memory.

Mathews fails to teach claim 6, which states "The method of claim 1 wherein determining the rank of page type in step (e) utilizes a sorting method of a 2-bit counter." However, McFarland's invention discloses "The circuitry includes a 2-bit counter 305, associated with which are flip-flops 307 and 308 whose clocked values represent bits 0 and 1 of the write address pointer" (Column 29, lines 66-67 and Column 30, lines 1-2). It would have been obvious to one of ordinary skill in the art, having the teachings of the "System and Method for Translation Buffer Accommodating Multiple Page Sizes" of Mathews and McFarland's "Improved Terminator for High Data Bus" before him at the time the invention was made, to combine the inventions to include a 2-bit counter for determining the rank of a page rank so that the system would run efficiently and so that the rank determination was more accurate.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658 and fax number is (571)273-1658. The examiner can normally be reached on M-Th, from 8-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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